Paradigm shift in packaging technology

2007. 5. 9

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IPT Team (SYS.LSI)
Contents

1. Packaging
   - Definition, Role, Mission

2. Paradigm shift
   - Mega-Trends, Challenges, Value Adding
   - Miniaturization, Integration/ High-density, High-performance

3. SiP Technology
   - Case study
   - Key technology and Infra-structure
   - Considerations
   - Roadmap
Signal Integrity, Power Integrity

Early Engagement
Floorplan
IR Drop Analysis
Place & Routing
RC Extraction with Coupling Cap.
Delay Calculation with Crosstalk Effect
IR Drop Analysis
Noise Analysis
OK
Post Layout Processing
PG Out

sa-pin File

SSN Analysis
Net-list

Preliminary Analysis (ScorpiO-QS or PS)

STA Simulation

ECO

ECO

Post Analysis

Constraint

Package Design

Preliminary Package Circuit Model

Post-Simulation; Circuit Model Extraction

Circuit Model (SPICE) ➔ Power Delivery Model ➔ Signal Delivery Model

Chip - Level

Package - Level
Thermal Design

- **Detail Modeling Simulation**
  - Package Level Detail Modeling
  - Physical Design Importing System
  - Leakage Power Curve (Worst/Average)

- **Application Set Thermal Environment**
  - Co-design of Package-level and Set-level Modeling
  - Set Environment Information
  - Standardization of STM (Set-level Thermal Model)

- **Technology to be Improved**
  - One-shot Design Guide relating Preliminary Design
  - Data Correlation with Simulation/Measurement
  - Design Verification System with Thermal
- DDR memory is weakest die. $T_j$ max = 85°C
- Ambient temperature ($T_a$) and Logic power should be controlled as $T_j < 85°C$.
- POP has better thermal performance than SIP.
Reliability Assessment

Accelerated Life Testing

- Temperature
- Humidity
- Voltage
- Contaminants
- Vibration

Different Acceleration Limits Can Give Different Result
Environmental Reliability Testing

- Pre-conditioning
- TC (Temperature Cycling)
- PCT (Pressure Cooker Test)
- Unbiased HAST
- THB (Temperature, Humidity & Bias Test)
- HTS (High Temperature Storage Test)
- 2-nd Level (Board Level Testing) : Drop, Bending
Key packaging process, materials, and equipment

- **Wafer Thinning and Stress Relief**
  - **Trends, Outlook**
    - Samsung ready to produce the SiP which contains less than 50umt die.
    - New technologies are need to be developed to enhance die strength and to protect die from environmentals.
  - **Challenges and Solutions**
    - Mechanical Issue: Wafer/Die Broken during Packaging Process
    - Electrical Issue: Electrical Issue might be happened, which is dependent on quality of back-grind and stress relief processes

### Wafer Thickness Roadmap (Samsung)

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>80um</td>
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<td></td>
<td>Mass Product</td>
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<td>70um</td>
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<td></td>
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<td>Special Product</td>
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<td>60um</td>
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<td></td>
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<tr>
<td>20um</td>
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<td>10um</td>
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<td></td>
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<td></td>
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</table>

### Key packaging processes, materials, and equipment

<table>
<thead>
<tr>
<th>Process (Chemical Mechanical polishing)</th>
<th>Wet Etching</th>
<th>Dry Etching (Plasma)</th>
<th>Dry Polishing</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reacting Substance</td>
<td>Slurry</td>
<td>HF + HNO₃</td>
<td>Oxidized metal abrasive</td>
</tr>
<tr>
<td>Processing rate</td>
<td>1 µm/min</td>
<td>&gt; 10 µm/min</td>
<td>2 µm/min</td>
</tr>
<tr>
<td>Productivity</td>
<td>Good</td>
<td>Excellent</td>
<td>Good</td>
</tr>
<tr>
<td>Die strength</td>
<td>Good</td>
<td>Good</td>
<td>Good</td>
</tr>
<tr>
<td>Environmental condition</td>
<td>Slurry management required</td>
<td>Generates NOx</td>
<td>SFE</td>
</tr>
<tr>
<td>Running cost</td>
<td>Acceptable</td>
<td>Acceptable</td>
<td>Acceptable</td>
</tr>
</tbody>
</table>

* Source: Disco
Stress Induced by Packaging

- Transistor shift by packaging stress ???
Key packaging process, materials, and equipment

- Laser Dicing
  - Trends, Outlook
    - Laser Dicing is needed for less than 50umt chip
  - Challenges and Solutions
    - Low Die Strength
      - Optimization of laser equipment and process or add an additional process such as plasma etching after laser dicing.
    - DAF Material Cutting
      - Collaboration among semiconductor co., laser equipment co., and material developing co.

Die Strength Comparison among Blade and various Laser

SEM Image of Stealth Laser Diced Wafer
Key packaging process, materials, and equipment

- Die Stacking Capability
  - Status in Samsung
    - 16 Chip in 1.6mm (’07) ← 10 Chip in 1.4mm (’06) ← 8 Chip in 1.4mm (’05)
  - Technical Issues
    - Back-grind; Stress Relief Process Equipment for under 30umt Water.
Key packaging process, materials, and equipment

- Interconnection; (1) Wire Bonding
  - Trends, Outlook
    - Fine Pad Pitch, Long Wire
    - Low Cost Solution for Cu BEOL Interconnection
  - Challenges and Solutions
    - Pad Pitch and Wire Sweeping → Wire Coating after WB or Using Coated Wire
    - WB Technology on Cu Pad Metal → E’less Ni/Au on Cu Pad, Cu Wire Bond
Key packaging process, materials, and equipment

- Interconnection; (2) Flip Chip

  - Trends, Outlook
    - Au-Stud Bump Technology in WB Designed Device
    - Solder Bump Technology in High Pin Count Device
    - Thin Package by Flip Chip Technology

  - Challenges and Solutions
    - Low Cost Flip Chip Technology → Substrate Technology, Pad Finish
    - Wafer Level Flip Chip Package for SiP such as Solder Bump Flip Chip
    - Fine Pitch Bumping Technology

High End 1296 HFC BGA

Solder Bump

Flip Chip BGA

From Semiconductor Insights
Key packaging process, materials, and equipment

- Interconnection; RDL / WLP
  - **Driving Force**
    - RDL: Customized Pad Allocation
    - WFP: Small Form Factor, High Electrical Performance
  - **Technical Issues**
    - Wafer-Level Test (KGD)
    - Handling & Shipping
    - Module Level Solder Joint Reliability without Underfill

60WLP based 512MB UDIMM

64WLP based 2GB SoDIMM

12” Wafer after WLP Process
Wafer Level Fabricated Package

- Real Chip Sized Package
- Wafer Level Manufacturing
Wafer Level Fabricated Packaging

- **ILD1**: Die Redistribution Layer Capacitance 5 ~ 20um
  - PSPI, PBO, BCB
  - 50um

- **Redistribution Layer**: I/O Pad Pitch Solder Ball
  - Die Redistribution Layout 5um
  - Seed Metal: PVD
  - Seed Metal Etch: Wet Etch

- **ILD2**: Solder Ball Attach Ball Land, 300 ~ 500um (450um)
- **BSP Film**: Back-Side Protection Film 50um

- **Solder Ball**: Die Substrate 300 ~ 500um (450um)
## Wafer Level Fabricated Packaging

### Process Flow

1. **Fab-outed wafer**
2. **ILD1 pattern**
3. **Seed metal depo. [Ti/Cu] / PR pattern**
4. **Electroplating [Cu / Ni]**
5. **PR strip / Seed metal etch**
6. **ILD 2 pattern**
7. **B/L , BSP Film Lamination**
8. **Ball attach / Reflow**
Bumping

1. Sputter
2. PR-Coating
3. Develop
4. Dry etch
5. EP. Ni
6. Plating
7. PR strip
8. UBM etch
9. Flux coating
10. Reflow
11. Cleaning
Key packaging process, materials, and equipment

packaging materials

EMC
- Low k Dielectric
- Narrow Gap Fill
- Warpage Control
- Halogen Free

Substrate
- Thinner Substrate
- Low CTE CCL
- Low k Dielectric
- Low Warpage
- High Reliability
- High Stiffness
- Halogen Free

Solder Ball
- Pb-free
- Fine Pitch Soldering
- Joint Reliability

Underfill
- Narrow Gap Filling (< 30um)
- Low Moisture Absorption
- High Adhesion

DAF
- High Adhesion
- Void Control
- Thermal Conductivity
Key packaging process, materials, and equipment

• Die Attach Film
  - Trends, Outlook
    - Thinner Die Attach Film ( <10um)
    - Wire Penetration Film & Good Gap Filling Film
    - Wafer Backside Direct Coating
    - Laser Dicing Film (Stealth Dicing)

  - Challenges & Solution
    - High Reliability → Void Free DAF
    - Thin DAF Materials → under 10um, under 50um
    - High Thermal Non Conductive DAF → Above 3~5mw/mk
    - Low Cost Solution → Wafer Backside Direct Coating
Key packaging process, materials, and equipment

• Substrate
  - Trends, Outlook
    ➢ Thinner Substrate
    ➢ Low k (65nm, 45nm, 32nm…)
      ➢ Low Stress (Low CTE, Low Warpage, Low Modulus, Fine Pitch)
    ➢ Environmental Friendly (Lead Free, Halogen Free)

- Challenges & Solution
  ➢ High Reliability ➢ High Adhesion & Low Moisture Absorption SR
  ➢ Thin Core Substrate ➢ Below 40um CCL (2-Layer 80um, 4-Layer 150um)
  ➢ Low Warpage ➢ Low CTE (Under 12ppm for Package)
Key packaging process, materials, and equipment

- **Equipments**
  
  - **Status in Samsung**
    
    - New Concept of Equipment is the KEY for Developing New Package
    

- **Technical Issues**
  
  - Back-grind; Stress Relief Process Equipment for under 30umt Water
  - Dicing; High Die Strength Laser Equipment
  - Thin Wafer Handling; Auto In-line Process, Low Cost, Simple Process
  - Die Pick-up; Damage-less Pick-up, High Speed
  - Encapsulation; Stress Free Large Area Molding
Key packaging process, materials, and equipment

- Equipments: 3D Vision
  - Status in Samsung
    - Outside Ball Vision & Leaded Package 3D Vision
      → Ball Coplanarity, Ball Height, Ball Pitch, Ball Damage, Missing Ball
  - Technical Issues
    - Stack Package Insider Ball Vision; Solder Joint Quality
      → X-Ray, IR Camera: Is Possible Sample Test Only (Long Test Time)
      → Mess Product 3D Vision?

Solder Ball Image Sample

Gap Measurement
PoP Development Direction

PoP (Wire-Bonding)
- Small Form-factor
- 14X14X1.4mm3

WSP (Wafer Stacked Package)
- Small Form-factor
- High-Speed

PoP (Flip-chip)
- High Speed
- Wide Bus
- 12X12X1.4mm3

IEP (IC-Embedded)
- 10X10X1.2mm3

CoC (Chip-on-Chip)
Flip-chip Benefit

1. MCP Ball Count:
   - Max. 128ea @ 0.65mm Pitch
   - Max. 168ea @ 0.50mm Pitch
2. PoP Ball Count:
   - Max. 457ea @ 0.50mm Pitch
   - 556ea @ 0.40mm Pitch
3. Die Size
   - Max. 6.50 x 6.50mm (WB Type)
   - Max. 8.00 x 8.00mm (FC Type)
4. Die Pad Count
   - Max. 350ea @ In-Line, 50um BPP
   - Max. 504ea @ Flip-chip 180um

14x14, WB-PoP, 1.5mm t

1. MCP Ball Count:
   - 152ea @ 0.65mm Pitch
   - 119ea @ 0.80mm Pitch
2. PoP Ball Count
   - 491 @ 0.50mm Pitch
3. Die Size
   - Max. 8.20 x 8.20mm
4. Die Pad Count
   - Max. 480ea @ In-Line, 50um BPP
Bottle Neck in High-end Phone

What will be the performance bottleneck in the future?
Wide Bus (Chip-on-Chip)

- Application CPU
- Memory Ctrl
- L3 Cache
- AMBA
- CPU1
- CPU2
- 3D-E
- DSP
- DRAM
- NVM
-DRAM
- NVM

- Bump Pad
- Wire Bonding Pad
- Power line

60㎛ Bump Pitch
15㎛ Passivation Open
30㎛ Bump Dia.
Sn-Ag solder (5㎛)
Cu or Ni bump (3㎛ ↑)

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Next Gen Technology: Embedded IC

- LSI Embedded PCB for PoP Application
  - Size reduction
  - Bunch of I/O placement between CPU and MCP
  - Bump Pitch: 200um, 180um
  - Daisy Chain, Functional Sample Build
Next Gen Technology: Through Si Via (TSV)

High-Density Memory

Through Via Fabrication

Via Filling

Device Chips

560um

Wafer Thinning

High-Accuracy Bonding
Next Gen Technology: Through Si Via (TSV)

Wafer Level Camera Module

- Ni Bump: Pad Stopper for Laser
- Patterned adhesive: Film lamination
- Glass attach & BSG: BS grinding,100um
- Si via formation: 1st YAG Laser Drilling
- Via insulation: Film laminate
- Resin ablation: 2nd YAG Laser Drilling
- RDL Process: ~10um
- SR Pad
- Ball Attach

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SiP Testing: Challenges and Solution

- **SiP Testing Environment**
  - Complexity
    - Logic, mixed signal, and large high speed memory at the same time
    - Smaller access pins than the sum of separate devices

- **Efficient testing for yield, quality, and productivity**
  - Parallel test for productivity
  - More testing at wafer level
    - Prevent yield loss at package level
  - Multiple or intermediate testing during the manufacturing flow
    - More chance of damages induced by testing
    - Optimize steps and skip test items Continuously

- **BIST (build-in self test) for DFT**
  - Reducing external pin count helps simple routing
  - To secure quality guarantee and failure analyses is challenging
  - Optimize I/O driving size
Considerations in SiP testing

- **Test Flow Planning**
  - SiP & PoP Test Flow Plan
  - Application Segment & Quality
  - BiST or DA mode for Memory
  - Memory Re-Charac on SiP

- **Test Coverage**
  - Test Escape
    - Physical & Electrical
  - Scenario Based Test
    - Characterization for Potential Failure

- **Pre-Screen for Yield-up**
  - Pre-screen of Interposer O/S
  - RF Testability on Wafer
## Various test circuit design

<table>
<thead>
<tr>
<th>Pinout Type</th>
<th>Separate Direct Access Mode</th>
<th>Shared Pin Direct Access Mode</th>
<th>Bypass Test Mode</th>
<th>BIST Test Mode</th>
</tr>
</thead>
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<tr>
<td>[Diagram]</td>
<td><img src="image1" alt="Separate Direct Access Mode" /></td>
<td><img src="image2" alt="Shared Pin Direct Access Mode" /></td>
<td><img src="image3" alt="Bypass Test Mode" /></td>
<td><img src="image4" alt="BIST Test Mode" /></td>
</tr>
</tbody>
</table>

**Pros.**
- Easy & Simple
- Signal pin share
- Reduced Pinout
- Smaller Package Size
- min. Pinout
- Smallest Package

**Cons.**
- PKG size increase
- Tri-state I/O required
- DFT in Logic
- Delay Skew Matching
- I/O Compatibility at Memory Burn_In
- Memory BIST in Logic
- Memory FA Difficulty

---

S : Signal  
P : Power (VDD)  
G : Power (GND)
PoP Test Flow Optimization

- **Memory MCP Test**
  - No Test after Stack, basically
  - No Burn-in on PoP even for Automotive (Single PPM Application)

- **Problem Areas**
  - PoP Stack Failure Detection
  - PoP Detach for Re-use

- **Future Expectation**
  - Low Pressure Test for Top PKG
    - TDA Feature Support
  - Standardization for MCP Ball Array, Physical Dimension, Ball Pitch, etc
  - Easy Rework Process for Re-use
Test flow for die stacked SiP

- **Memory B/I Test**
  - Generally, no B/I with KGD
  - B/I required for Automotive or Single PPM Application

- **Problem Areas**
  - Wafer Screen for Potential Loss
  - Speed & Ids Bin Balance
  - One of Any Dies Fail, then Lose All
  - Interposer O/S Detection
  - BiST Support B/I Equipment
  - After all, High Yield Loss

- **Future Expectation**
  - In Situ O/S Test during Assembly
  - Test Infra before Molding Step
  - Performance Test on Wafer
3-D integration outlook

● SiP is more practical than SoC:
  - High density integration, Variety of function (memory, passive, analog, mems, etc.)
  - Time to market, low cost
  - Flexibility in changes and options
  - Moderate performance (band width, interface speed)

● Die stacking vs. Package stacking (PoP)
  - PoP advantages are:
    ✓ Flexibility in memory options, generation shift, manufacturing flow & logistics
    ✓ Tested memory guarantee high cumulative yield
    ✓ Challenges: warpage control, 2-nd level reliability, small form-factor
  - Die Stacking has advantages of:
    ✓ Proprietry differentiated total solution, total IP block (Black-box), strong entry barrier
    ✓ Relatively small form-factor
    ✓ Challenges: yield management (KGD, DFT), change management

- Future technology outlook
  ✓ TSV stacking seems ultimate solution: more than 3-dies, low RLC delay, small form-factor
Considerations in SiP Planning

- Know requirements from set-maker: (1)
  - Die Combination, form-factor budget, Thermal/electrical constraints

- Low cost design-In: high yield, cheaper materials, min. investment
  - SiP friendly chip design (chip – package co-design) (2)
  - DFT, efficient test flow (1)
  - Low cost PCB (1)
  - High yield: KGD, package yield. (1)

- Simple Logistics, efficient manufacturing (1)

- Quality control and failure analyses (collaboration, liability)

→ Low cost, small size, and high-density
Considerations in SiP Planning

- Know customers requirements, and driving force.

  - **What is driving force for SiP**
    - Form-factor
    - Low cost BOM
    - Functionality gain
    - Simple Logistics
    - Others

  - **Know boundary conditions:**
    - Form-factor budget
    - Electrical, thermal requirements, and boundary conditions
    - Set board information and reliability conditions
    - 2-nd level reliability test methods and criteria.
    - Failure analyses, rework SOP
    - Quality control level (in process, field fail rate)
Considerations in SiP Planning

- Low cost design-In
  - PCB is dominant material cost
    ✓ Plan small size SiP (increase PCB usage)
    ✓ Simplify PCB design
      - Reduce design complexity: SiP friendly chip design, reduce pin-count, use interposer
  - Minimize yield loss
    ✓ Avoiding external memory testing
    ✓ Use tested memory (PoP) or KGD (die stacking)
    ✓ Increase wafer sorting coverage
    ✓ Use DFT or self-testing circuit
    ✓ Get high assembly yield
## Package Stack Technology Roadmap

### Year
<table>
<thead>
<tr>
<th></th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Total Height (in Typical)</strong>&lt;sup&gt;①&lt;/sup&gt;</td>
<td>1.6mm</td>
<td>1.4mm</td>
<td>1.2mm</td>
<td>1.0mm</td>
</tr>
<tr>
<td><strong>Logic Package</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mold / FC</td>
<td>0.30/-</td>
<td>0.27/0.16</td>
<td>0.25/0.10</td>
<td>0.23/0.08</td>
</tr>
<tr>
<td>Chip Thickness</td>
<td>0.08/-</td>
<td>0.05/0.10</td>
<td>0.05/0.08</td>
<td>0.03/0.06</td>
</tr>
<tr>
<td>PCB (4L)</td>
<td>0.30</td>
<td>0.22</td>
<td>0.22</td>
<td>0.18</td>
</tr>
<tr>
<td>Ball Height (0.5 Pitch)</td>
<td>0.24</td>
<td>0.24</td>
<td>0.15</td>
<td>0.00 (LGA)</td>
</tr>
<tr>
<td><strong>MCP (2 Chip)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mold / Chip Thickness</td>
<td>0.45/0.08</td>
<td>0.35/0.05</td>
<td>0.30/0.05</td>
<td>0.25/0.03</td>
</tr>
<tr>
<td>PCB (2L)</td>
<td>0.13</td>
<td>0.13</td>
<td>0.11</td>
<td>0.08</td>
</tr>
<tr>
<td><strong>Solder Joint Height</strong>&lt;sup&gt;②&lt;/sup&gt;</td>
<td>0.35/0.26</td>
<td>0.32/0.21</td>
<td>0.30/0.15</td>
<td>0.28/0.13</td>
</tr>
</tbody>
</table>

---

<sup>①</sup> *Total Height in Typical, MCP in 2-Same Die, Logic : 1-Chip in Staggered Pads*

<sup>②</sup> *Clearance between top and bottom package : um*
### Die Stack Technology Roadmap

![Die Stack Technology Diagram](image)

#### Year 2005 2006 2007 2008

<table>
<thead>
<tr>
<th>Total Height (4-Chip/Production)</th>
<th>1.4mm</th>
<th>1.2mm</th>
<th>1.0mm</th>
<th>0.8mm</th>
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<tbody>
<tr>
<td>Mold</td>
<td>0.80</td>
<td>0.70</td>
<td>0.55</td>
<td>0.50</td>
</tr>
<tr>
<td>Chip</td>
<td>0.08</td>
<td>0.08</td>
<td>0.05</td>
<td>0.05</td>
</tr>
<tr>
<td>Adhesive</td>
<td>0.02</td>
<td>0.02</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Spacer</td>
<td>Si 0.08</td>
<td>Si 0.08</td>
<td>Tape 0.06</td>
<td>Tape 0.06</td>
</tr>
<tr>
<td>PCB (4L)</td>
<td>0.26</td>
<td>0.22</td>
<td>0.22</td>
<td>0.22</td>
</tr>
<tr>
<td>Solder Ball Height (0.5 Pitch)</td>
<td>0.24</td>
<td>0.24</td>
<td>0.20</td>
<td>0.00 (LGA)</td>
</tr>
</tbody>
</table>
IPT Roadmap

Year ~2001 2003 2004 2005 2006 2007 2008

High Performance BGA
- FC-BGA
- CDG
- COF
- TEBGA
- Build-up
- UELP 0.5t
- PoP Flip-chip
- Embedded
- 3D Opto-Electric Integration

High Density SIP
- FBGA 1.2t
- LQFP/E
- TEBGA
- HBGA
- High Pin BGA
- LQFP 1.4t
- TBGA 1.2t

Card/Module
- FBGA 1.4t
- ELP 0.8t
- ULGA 0.5t
- CIS Module
- Glass Image Sensor
- WQFP 0.75t
- WLP
- COF
- COG

Standard Package
- Small Size & High Density
- Integrated Product Stack/SIP
- Intelligent System Integration

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